In the specification:

Please amend the paragraph beginning at page 6, line 16 as follows:

Code ordering means that the logical constructs are sorted based on producer/consumer relationships. That is, a logical construct representing an element that "produces" or outputs a signal is ordered before another element that "consumes" or receives the signal as an input. ~~BY~~ By subsequently code-ordering the C++ model may be simulated as a single call model. A single call model means that each logical construct is evaluated only once per cycle. Hence, the C++ model simulator is a cycle-based simulator. The Verilog model is also written after being extracted from the data structure and is typically simulated using an event driven simulator such as ModelSim™ from Model Technology, for example.

A1